Parallel Port Controller

Figures

Description

The parallel port allows the attachment of devices that transfer eight bits of parallel data at standard transistor-transistor levels. It has a 25-pin, D-shell connector. The primary function of the parallel port is to attach a printer with a parallel interface to the system. The parallel port function consists of the controller and the connectors.

There are three types of parallel port controllers: Type 1, Type 2, and Type 3. The type number indicates the function provided in the controller. The address of each controller can be configured and set to 1, 2, or 3 for Type 1 and Type 2 controllers. The address can be set to 1, 2, 3, or 4 for Type 3 controller.

The parallel port controller has an extended mode that supports bidirectional input and output. All three types support bidirectional input and output. In addition, Type 2 and Type 3 parallel port controllers support DMA transfers when in this mode. During power-on self-test the Type 2 and Type 3 controllers are put into extended mode so that DMA is available (See Programming Considerations on page 3). The parallel port controller supports level-sensitive interrupts and a readable interrupt-pending status indicator.

The following figure is a block diagram of the parallel port controller.

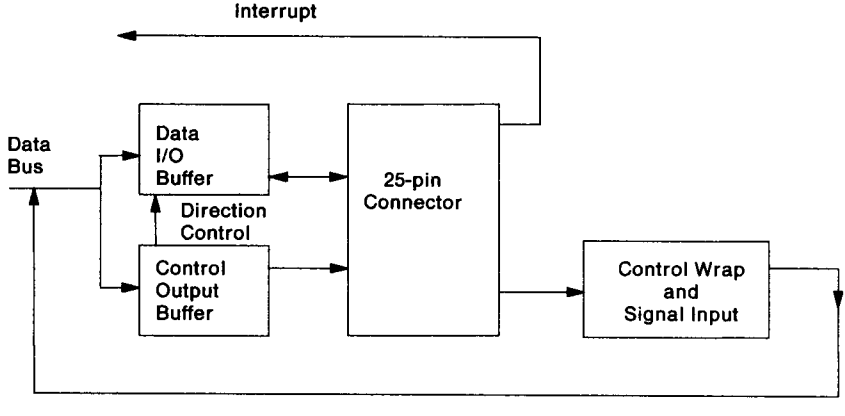


Figure 1. Parallel Port Controller

Programmable Option Select

This section describes the address selection, the extended mode, and DMA arbitration for the parallel port controllers.

Address Selection

The parallel port can be configured to the customary three addresses used by IBM Personal Computer products. These addresses are selected through programmable option select (POS) registers during system board setup.

The address assignments for each configuration are shown in the following tables. All addresses are in hexadecimal.

Port Number	Parallel Data Register	Device Status Register	Device Control Register	Reserved Register	IRQ
Parallel 1	03BC	03BD	03BE	03BF	7
Parallel 2	0378	0379	037A	037B	7
Parallel 3	0278	0279	027A	027B	7

Figure 2. Address Assignments (Type 1)

Port Number	Parallel Data Register	Device Status Register	Device Control Register	Interface Control Register	Interface Status Register	Reserved Register	IRQ
Parallel 1*	03BC	03BD	03BE	03BF			7
Parallel 2	0378	0379	037A	037B	037C	037D	7
Parallel 3	0278	0279	027A	027B	027C	027D	7

*Type 2 controllers do not support DMA on parallel port 1.

Figure 3. Address Assignments (Type 2)

Port Number	Parallel Data Register	Device Status Register	Device Control Register	Interface Control Register	Interface Status Register	Reserved Register	IRQ
Parallel 1*	03BC*	03BD*	03BE*	03BF*			7
Parallel 1	1278	1279	127A	127B	127C	127D	7
Parallel 2	0378	0379	037A	037B	037C	037D	7
Parallel 3	0278	0279	027A	027B	027C	027D	7
Parallel 4	1378	1379	137A	137B	137C	137D	7

*These addresses are for compatibility. To use full function, set the address range to start at hex 1278.

Figure 4. Address Assignments (Type 3)

Extended Mode

The extended mode option is selected through the POS function during system board setup. The extended mode makes the parallel port an 8-bit parallel bidirectional interface and makes DMA available for Type 2 and Type 3 controllers. The parallel port provides half duplex transfers when in bidirectional operation mode. Direction is determined by bit 5 of the Device Control register and DMA is controlled through the Interface Control register.

Arbitration Level (Type 2 and Type 3)

The Type 2 controller is fixed at arbitration level 6 and cannot be set through POS. The Type 3 controller allows arbitration levels to be configured to any level through the POS function.

Parallel Port Controller Programming Considerations

The following are some considerations for programming the parallel port controller.

The interface has three registers that respond to input and output instructions. The three registers are:

- A read and write Parallel Data register
- A read only Device Status register
- A read and write Device Control register.

The Type 2 and Type 3 controllers have three additional registers:

- A read and write Interface Control register
- A read only Interface Status register
- A write only Reserved register.

These registers are available in extended mode only.

During POST the parallel port is configured as an output port. POST status information is written to this port during the power-on initialization or the initialization caused by a reset from the keyboard (Ctrl + Alt + Del).

DMA Mode (Type 2 and Type 3 Only)

Single DMA transfers are supported both when sending and receiving. The DMA enable bit in the Interface Control register is set to 1 when DMA service is requested.

The parallel port has two idle states while it is in the DMA mode:

- Not ready (end-of-data bit = 1): Any request generates an interrupt if the interrupt is enabled. This state is entered after completing a DMA transfer or after setting the End of Data bit (bit 6) in the Interface Control register to 1.
- Ready (end-of-data bit = 0): While in this state, a pulse on the '-acknowledge' signal starts a DMA transfer. This state is entered after the Start DMA bit or the Reset End of Data bit (bit 6) is set in the Interface Control register to 1.

In addition, there are two data transfer states:

- Send byte: This state is entered when bit 5 of the Device Control register is set to 0 and a Start DMA or an '-acknowledge' signal is set. A DMA fetch transfer is initiated, the data is placed on the interface, and the 'strobe' signal line is pulsed.
- Receive byte: This state is entered when the direction bit is set to 1 and an '-acknowledge' signal is set. A DMA store is initiated and the 'strobe' signal is pulsed to acknowledge the completion of the operation. The incoming data is latched at the trailing edge of the '-acknowledge' signal.

Sending

Writing a 1 to the start-DMA bit in the Interface Control register initiates the DMA transfer to the attached device. (The enable DMA bit must have been set to 1 in a previous operation). The DMA Controller channel and the direction of the transfer are set before writing a 1 to the start-DMA bit. If the device is not busy, the parallel port controller requests the system bus. After control of the bus is gained, the following sequence of events occur:

1. Data is read from memory and written to the Parallel Data register by the DMA controller.
2. Data is carried to the attached device using the 'strobe' signal on the parallel interface.
3. The 'strobe' signal is activated automatically after the Parallel Data register is written.
4. The device issues the '-acknowledge' signal when the data transmission is completed.

Note: The '-acknowledge ' signal is used to trigger the next DMA transfer, if the end-of-data latch (bit 6 of the Interface Status register equals 0) is reset and DMA is enabled. In addition, the attached device must hold the 'busy' signal inactive for the parallel port to issue a DMA request.

When a terminal count is reached during a DMA transfer, the end-of-data latch is set and the next DMA transfer is prevented. It is known that the DMA controller has transferred the last byte of data to the parallel port controller. However, it is not known if the attached device has received the last byte of data. The parallel port controller is designed to interrupt at the '-acknowledge' signal after the end-of-data latch is set. At the completion of a DMA transfer, the parallel port controller will interrupt if the terminal-count interrupt-enable bit is set.

By setting the end-of-data (EOD) bit in the Interface Control register, the current DMA operation will be terminated. It should be noted that no interrupt will be generated by setting this bit.

This causes an effect similar to terminal count. One additional byte of data may be sent depending on the timing of the setting of the bit.

Disabling the DMA while a DMA transfer is in progress stops the generation of 'strobe' signals and causes an interrupt to end the DMA transfer.

Receiving

The DMA channel must be initialized prior to receiving data from the attached device. When the parallel port controller is ready to receive data from the attached device, the parallel port controller uses the '-acknowledge' signal. The '-acknowledge' signal initiates the DMA transfer to the system memory, if the end-of-data latch is reset and DMA is enabled. Data transmission allows the parallel port controller to request the system bus. After control of the bus is gained, the following sequence of events occur:

1. Data in the Parallel Data register of the parallel port controller is read and then written to memory by the DMA controller.
2. The 'strobe' signal is activated after the read command pulse to the Parallel Data register.

The parallel port controller cannot receive subsequent data until the previous data has been read by the DMA controller and transferred to the system memory. When the '-acknowledge' signal goes low, (data is being placed on the bus) the parallel port controller asserts the '-autofeed' signal (-AUTOFD) line high to inform the attached device of a busy state. After the DMA controller reads the data from the Parallel Data register, a 'strobe' signal is generated automatically as an acknowledgement of data transmission. A positive edge of the 'strobe' signal resets the -AUTOFD line low to tell the attached device that the controller is not busy. The 'busy' signal has no effect in receive mode.

To determine the end of a DMA transfer, the parallel port controller interrupts if the terminal-count interrupt-enable bit is on. When the terminal count is reached during a DMA transfer, the end-of-data latch is set to prevent the next DMA cycle and an interrupt occurs. The DMA controller has transferred the last byte of data to the memory.

Interrupt Condition

When enabled, the following event can cause an interrupt:

- Any transition of the '-error' signal
- Any transition of the 'paper end' signal
- Any transition of the 'select' signal

- The positive edge of the '-acknowledge' signal
  - When DMA is disabled
  - When DMA is enabled and end-of-data is set
- Terminal count while DMA is enabled while receiving.

Output Data Rate

The approximate time between two data bytes in a DMA operation is 5 microseconds, assuming that the attached device returns the '-acknowledge' signal to the 'strobe' signal immediately. In addition, the '-acknowledge' signal is 1.0 microseconds wide (the '-acknowledge' signal falls low and not later than approximately 1.0 microseconds after the rising edge of the '-strobe' line). To calculate the data rate, the delay from the '-strobe' signal to the '-acknowledge' signal on the attached device side should be added for each transmission. The transfer rate varies according to the DMA channel usage of the system.

Register Definitions

The following definitions apply to all types of parallel port controllers, unless specified otherwise. All reserved bits will be written as 0, and read as a 1.

Parallel Data Register

The Parallel Data register is a read and write register. Its output drivers are enabled by the direction bit in the Device Control register. A read operation returns the output data, if the output drivers are enabled or if data is read from the attached device when the drivers are not enabled. Care must be taken not to enable the drivers when the attached device is also driving the interface.

CAUTION:
Damage to the system can occur if the controller and the attached device are driving data onto the data lines at the same time. Therefore, do not enable the drivers when the attached device is driving the interface.

The Parallel Data register is an 8-bit data register for both the compatible and extended modes. In compatible mode, writing to this

register immediately presents data to the connector. Reading this register returns the last byte written.

In extended mode, writing to this register latches the data; however, the data is presented to the connector only if the direction bit is 0 (write). Reading the register returns either:

- The last byte written, if the direction bit is 0
- The data on the connector from the attached device, if the direction bit is 1.

Bit	Description
7 - 0	Data

Figure 5. Parallel Data Register

Bits 7 - 0 These bits represent the data (D7 - D0) on the signal lines of the connector.

Device Status Register

This read-only register contains the status of the attached device and the status of the interrupt.

Note: Reading this register resets an interrupt latch caused by the '-acknowledge' signal. Because reading this register restores bit 2 (-IRQ STATUS) to 1, there is a small window where the rising edge of the 'acknowledge' signal can arrive at the same time that the register is being read. This prevents bit 2 from being set to 0 as it would have been without the read operation. This condition also prevents the associated interrupt if it was enabled in the Device Control Register.

This register returns the interrupt-pending status of the interface, and the real-time status of the connector pins, as shown in figure 6.

Bit	Description
7	-BUSY
6	-ACKNOWLEDGE
5	PAPER END
4	SELECT
3	-ERROR
2	-IRQ STATUS
1, 0	Reserved

Figure 6. Device Status Register

Bit 7 This bit represents the state of the '-busy' signal. When this bit is set to 0, the printer is busy and cannot accept data.

Bit 6 This bit represents the current state of the device '-acknowledge' signal. When this bit is pulsed, the device has received a character and is ready to accept another.

Bit 5 This bit represents the current state of the device 'paper end' signal. When this bit is set to 1, the printer has detected the end of the paper.

Bit 4 This bit represents the current state of the 'select' signal. When this bit is set to 1, the printer has been selected.

Bit 3 This bit represents the current state of the device '-error' signal. When this bit is set to 0, the printer has encountered an error condition.

Bit 2 This bit is set to 0 when the device has acknowledged the previous transfer using the '-acknowledge' signal. This bit is set to 1 when the Device Status register or the Interface Status register is read. An interrupt is pending when this bit is set to 0. This bit is used in non-DMA mode only.

Bits 1, 0 These bits are reserved.

Device Control Register

This is a read and write register that controls lines to the attached device. Reading this register returns the last byte written to the register, if the line is not driven by the attached device. The direction bit can be updated at any time, but the effect of the bit is masked when in non-extended mode (in compatible mode the direction is always out, even if the bit reads as 1).

Bit	Description
7, 6	Reserved
5	Direction
4	IRQ EN
3	SLCT IN
2	-INIT
1	AUTO FD XT
0	STROBE

Figure 7. Device Control Register (Type 1 and Type 2)

Bits 7, 6 These bits are reserved and must be set to 0. This bit always reads as 1.

Bit 5 This bit controls the direction of the data port. When this bit is set to 0, the data drivers are enabled and the parallel data is placed on the output data lines. A read operation will return a 1 for Type 1 and the last value written for Type 2.

Bit 4 This bit enables the parallel port interrupt. When this bit is set to 1, an interrupt occurs when the '-acknowledge' signal changes from active to inactive (non-DMA mode only).

Bit 3 This bit controls the 'select in' signal. When this bit is set to 1, the printer is selected.

Bit 2 This bit controls the 'initialize' signal. When this bit is set to 0, the printer will be initialized.

Bit 1 This bit controls the 'automatic feed XT' signal. When this bit is set to 1, the printer automatically spaces the paper up one line for every carriage return.

Bit 0 This bit controls the 'strobe' signal to the printer. When this bit is set to 1, data is clocked into the printer.

Bit	Description
7	Autostrobe
6	Reserved
5	Direction
4	IRQ Enable
3	SLCT IN
2	-INIT
1	AUTO FD XT
0	STROBE

Figure 8. Device Control Register (Type 3)

Bit 7 This bit, when set to 1, enables the 'Autostrobe' signal.

Bit 6 This bit is reserved and must be set to 1. A read operation will return a value of 1.

Bit 5 This bit controls the direction of the data register. When this bit is set to 0, the data drivers are enabled and the parallel data is placed on the output data lines. A read operation will return a 1 in non-extended mode and the last value written in extended mode.

Bit 4 This bit enables the parallel port interrupt. When this bit is set to 1, an interrupt occurs when the '-acknowledge' signal changes from active to inactive (non-DMA mode only).

Bit 3 This bit controls the 'select in' signal. When this bit is set to 1, the printer is selected.

Bit 2 This bit controls the 'initialize' signal. When this bit is set to 0, the printer will be initialized.

Bit 1 This bit controls the 'automatic feed XT' signal. When this bit is set to 1, the printer automatically spaces the paper up one line for every carriage return.

Bit 0 This bit controls the 'strobe' signal to the printer. When this bit is set to 1, data is clocked to the printer.

CAUTION:
Do not enable the drivers for the data lines while the attached device is driving them.

Interface Control Register

This register controls the various functions available in the interface. All bits read as 1 in non-extended mode. Bits 1, 6, and 7 always read as 1.

Bit	Description
7	Start DMA
6	Reset EOD
5	Enable TC/ACK Interrupt
4	SLCT IRQ Enable
3	-ERROR IRQ Enable
2	PE IRQ Enable
1	Set EOD
0	Enable DMA

Figure 9. Interface Control Register (Type 2 and Type 3)

Bit 7 Writing a 1 to this bit initiates a DMA transfer. The Enable DMA (bit 0) must have been set to 1 in a previous write operation, otherwise the results are indeterminate. Reading this bit always returns as a 1.

Bit 6 Setting this bit to 1 resets the end-of-data latch, which allows the port to honor DMA transfer requests by the '-acknowledge' signal. Reading this bit always returns a 1.

Bit 5 Setting the bit to 1 enables interrupts to occur whenever the terminal count is achieved, or whenever an '-acknowledge' signal occurs with the end-of-data latch set. A 0 clears the terminal count '-acknowledge' signal in the Interface Status register and removes any pending interrupts caused by the terminal count. This bit is used only in DMA mode.

Bit 4 This bit is valid in the extended mode and setting this bit to 1 enables interrupts to occur on either edge of SELECT. Resetting this bit clears the 'select interrupt request' signal (SLCT IRQ) in the Interface Status register.

Bit 3 This bit is valid in the extended mode and enables interrupts to occur on either edge of an '-error' signal. Resetting this bit clears the 'error interrupt request' signal (-ERROR IRQ) in the Interface Status register.

Bit 2 This bit is valid in the extended mode and enables interrupts to occur on either edge of a 'paper end' signal. Resetting this bit clears the 'paper end interrupt request' (PE IRQ) in the Interface Status register.

Bit 1 Setting this bit to 1 sets the end-of-data latch which will stop DMA transfers before terminal count is reached. Reading this bit always returns a 1. This output generates a pulse and always reads as 1.

Bit 0 This bit enables the DMA function. Whenever this bit is set from a reset condition, the end-of-data latch (bit 1) must also be set to prevent unknown states. The extended mode must be set in the POS register before this bit can be set.

Writing certain bit combinations of the Interface Control register may cause unexpected results. Those bit combinations listed as reserved in the following figure, must not be used.

Bits 7 6 1 0	Function
00 00	Reserved
00 01	No Change to DMA Operation
00 10	Disable DMA
00 11	Halt DMA or Enable DMA
01 00	Reserved
01 01	Set Ready-to-Start DMA in Receive Mode
01 10	Reserved
01 11	Reserved
10 00	Reserved
10 01	Start DMA in Send Mode
10 10	Reserved
10 11	Reserved
11 00	Reserved
11 01	Reserved
11 10	Reserved
11 11	Reserved

Figure 10. Interface Control Register DMA Functions

Interface Status Register

This is a read-only register and is used to convey the status of the parallel interface. Reading this register resets the interrupt pending status bits and resets the interrupt request. The interrupt handler must save the status or process it completely before returning. Disabling the interrupts with the Interface Control register also clears the corresponding interrupt-request bit. All bits in this register read as 1 in compatible mode.

Note: Because reading the register resets the interrupt status (bits 2 through 5), there is a small window where the interrupting condition, if it occurs at the end of the read operation, will not set the corresponding interrupt status bit (the interrupt is also prevented). A periodic check of the corresponding status bits in the Device Status register and the EOD bit in this register can be used to detect this condition.

Bit	Description
7	Reserved
6	EOD
5	TC/ACK Interrupt
4	SLCT Interrupt
3	Error Interrupt
2	PE Interrupt
1,0	Reserved

Figure 11. Interface Status Register (Type 2 and Type 3)

Bit 7 This bit is reserved.

Bit 6 When the EOD bit is 1, it indicates that the end-of-data latch is set and the parallel port is not ready to perform a DMA transfer. This occurs when the terminal count is reached or when the latch is set through the set-end-of-data-latch bit in the Interface Control register.

Bit 5 When the TC/ACK interrupt bit is set to 1, it indicates that the pending interrupt is caused by the terminal count or by an '-acknowledge' signal. If the EOD bit is 1, the interrupt was caused by the terminal count, otherwise it is caused by the 'acknowledge' signal.

Bit 4 When the SLCT interrupt bit is 1, it indicates that the pending interrupt is caused by any transition of the 'select' signal.

Bit 3 When the error interrupt bit is 1, it indicates that the pending interrupt is caused by any transition of the 'error' signal.

Bit 2 When the PE interrupt bit is set to 1, it indicates that the pending interrupt is caused by any transition of the 'paper end' signal.

Bit 1,0 These bits are reserved.

Reserved Register Initialization

This register must be loaded with a value of Hex 16 before using the DMA mode.

Reading this register gives unpredictable values.

Bit	Description
7 - 0	Must Be Hex 16

Figure 12. Reserved Register (Type 2 and 3)

Parallel Port Timing

Timing for the parallel port depends on the devices connected to the port. The following figure shows the minimum requirements for the parallel-port signal timing and any device that may be attached to the parallel port.

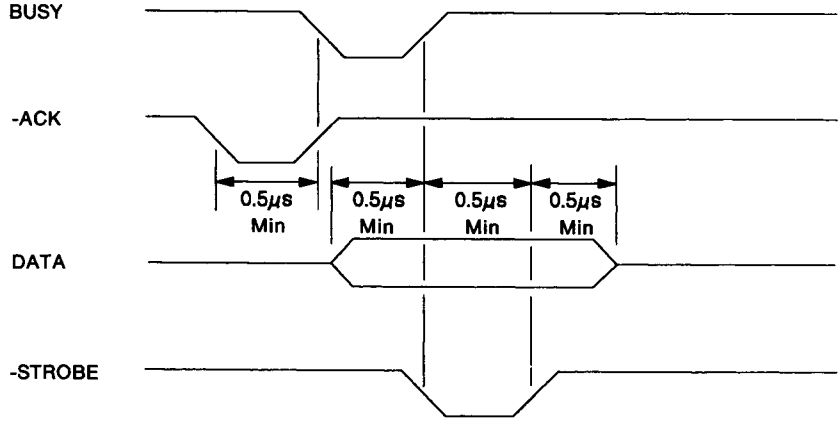


Figure 13. Parallel-Port Timing Sequence

The DMA (Types 2 and 3) and Autostrobe (Type 3) functions will generate these timings automatically. In sending modes, -STROBE will be activated 1.0 ±0.25 microseconds after the data is placed on the output data lines. The -STROBE pulse width is 1.0 ±0.25 microseconds. In DMA receive mode, a strobe pulse 1.0 ±0.25 microseconds wide will be generated as soon as the data has been read from the data lines.

For specific signal timing parameters, refer to the specifications for the equipment connected to the parallel port connector.

Signal Descriptions

The following figures, schematics, and tables, are representative circuits of the Parallel Port interface signals.

Parameter	Value	Limit
High-Level Input Voltage	2 V	Minimum
Low-Level Input Voltage	0.8 V	Maximum
High-Level Input Current	40 μA	Maximum
Low-Level Input Current	-0.8 mA	Maximum

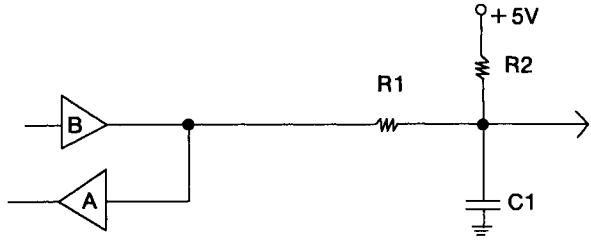
Figure 14. Receiver A Specifications

Parameter	Value	Limit
Sink Current	24 mA	Maximum
Source Current	-2.6 mA	Maximum
High-Level Output Voltage	2.4 Vdc	Minimum
Low-Level Output Voltage	0.5 Vdc	Maximum

Figure 15. Driver B Specifications

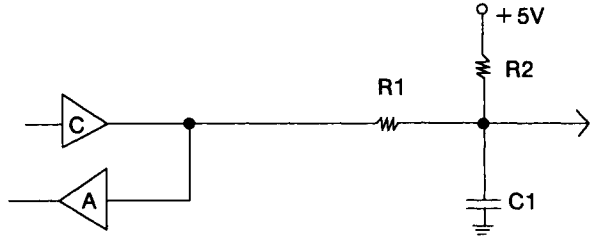
Parameter	Value	Limit
Sink Current	20 mA	Maximum
Source Current	Open Collector	
High-Level Output Voltage	Open Collector	
Low-Level Output Voltage	0.5 Vdc	Maximum

Figure 16. Driver C Specifications



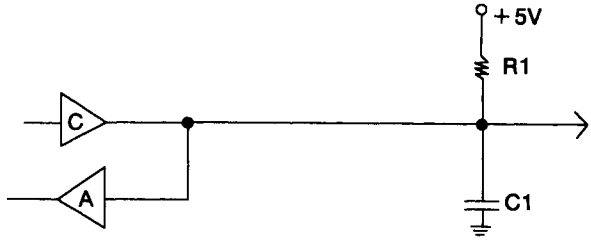
Symbol	Value
R 1	33 Ω
R 2	2 kilo ohms or Not Present
C 1	0.0022 μF or Not Present

Figure 17. Data Lines



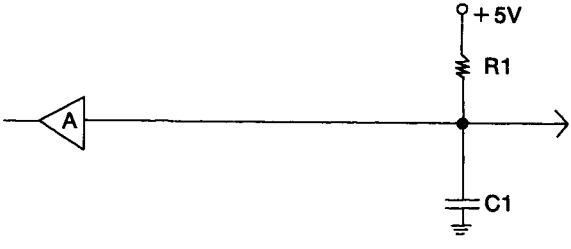
Symbol	Value
R 1	33 Ω
R 2	2 kilo ohms to 4.7 kilo ohms
C 1	0.0022 μF or Not Present

Figure 18. -STROBE



Symbol	Value
R 1	2 kilo ohms to 4.7 kilo ohms
C 1	0.0022 μF or Not Present

Figure 19. -AUTOFDXT, -INIT, -SLCTIN



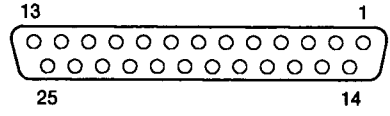
Symbol	Value
R 1	1 kilo ohms to 10 kilo ohms or Not Present
C 1	0.00068 to .0022 μF or Not Present

Figure 20. -ACK, BUSY, PE, SLCT, -ERROR

Connector

The parallel port connector is a standard 25-pin female D-shell connector.

The following figure shows the signal and pin assignments for the parallel port connector.



Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name
1	I/O	-STROBE	14	O	-AUTO FD XT
2	I/O	Data 0	15	I	-ERROR
3	I/O	Data 1	16	O	-INIT
4	I/O	Data 2	17	O	-SLCT IN
5	I/O	Data 3	18	NA	Ground
6	I/O	Data 4	19	NA	Ground
7	I/O	Data 5	20	NA	Ground
8	I/O	Data 6	21	NA	Ground
9	I/O	Data 7	22	NA	Ground
10	I	-ACK	23	NA	Ground
11	I	BUSY	24	NA	Ground
12	I	PE	25	NA	Ground
13	I	SLCT			

Figure 21. Parallel Port Connector Signal and Pin Assignments

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Notes: